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PATENT APPLICATION

ATTORNEY DOCKET NO. 10017481-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Blaine D. Gaither

Serial No.: 10/004,195 Examiner: Elmore, Reba I

Filing Date: 10/31/2001 Group Art Unit: 2187

Title: Computer performance improvement by adjusting a time used for preemptive eviction of cache entries

COMMISSIONER FOR PATENTS
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BRIEF ON APPEAL

INTRODUCTION

Pursuant to the provisions of 37 CFR Part 41, Subpart B, applicants hereby appeal to the Board of Patent Appeals and Interferences (the "Board") from the examiner's final rejection dated 11/10/2004. A notice of appeal was timely filed on 06/03/2005, in accordance with 37 CFR § 41.31(a)(1).

REAL PARTY IN INTEREST

The entire interest in the present application has been assigned to Hewlett-Packard Development Company, L.P. as recorded at reel 014061, frame 0492.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-8 are pending in the application.

Claims 1-8 are finally rejected.

Claims 1-8 are on appeal.

STATUS OF AMENDMENTS

There are no after-final amendments.

SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates generally to computer systems and more specifically to cache memory systems. In an example embodiment, the time used to determine when a cache memory line is stale is made dynamically variable (figure 4; page 11, lines 8-28). A computer system can adjust the time to optimize a measure of performance. In a first example, the performance measure is the rate of cache-to-cache transfers (figure 5; page 12, line 1, to page 13, line 6). In a second example, the performance measure is the rate at which evicted lines are reclaimed from an eviction queue (figure 6; page 13, line 7 to page 14, line 13).

Claim 1 specifies a method of improving performance of a computer system (figures 3 and 4), comprising: (a) specifying a time period (304, 402); (b) evicting, from a cache memory, at least one entry that has remained unchanged for at least the time period (310); (c) measuring at least one performance parameter (404); (d) changing the value of the time period (406); (e) repeating steps (b) and (c); and (f) determining whether the performance parameter has changed (412) (page 11, lines 8-28) .

Claim 2, dependent on claim 1, further specifies, step (c) further comprising measuring the rate of cache-to-cache transfers (figure 5; page 12, line 1, to page 13, line 6)

Claim 3, dependent on claim 1, further specifies, step (c) further comprising measuring how many evicted entries are accessed during a predetermined time span (figure 6; page 13, line 7 to page 14, line 13).

Claim 4, dependent on claim 1, further specifies, step (b) further comprising evicting, from a cache memory, at least one modified entry that has remained unchanged for at least the time period (figure 2B, 206).

Claim 5, dependent on claim 1, further specifies, step (b) further comprising evicting, from a cache memory, at least one entry that was received in a cache-to-cache transfer and has remained unchanged for at least the time period (figure 5; page 12, line 1, to page 13, line 6).

Claim 6, dependent on claim 1, further specifies, step (b) further comprising evicting, from a cache memory, at least one modified entry that was received in a cache-to-cache transfer and has remained unchanged for at least the time period (figure 5; page 12, line 1, to page 13, line 6).

Claim 7, dependent on claim 1, further specifies, repeating steps (a) through (f) until the performance parameter is optimized (figure 4, 406-412: page 11, lines 8-28).

Claim 8, dependent on claim 1, further specifies repeating steps (a) through (f) until the performance parameter changes (figure 4, 406-412: page 11, lines 8-28).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1-8 are unpatentable under the judicially created doctrine of obvious-type double patenting over U.S. Patent Number 6,813,691.

2. Whether claims 1-8 are unpatentable under the judicially created doctrine of obvious-type double patenting over copending U.S. Patent Application Number 10/001,586.

3. Whether claims 1, 3-4 and 7-8 are unpatentable under 35 U.S.C. § 102 as anticipated by U.S. Patent Number 6,678,794 (Talyansky *et al.*)

ARGUMENT

CLAIMS 1-8 IN LIGHT OF U.S. PATENT NUMBER 6,813,691.

Whether claims are unpatentable under the judicially created doctrine of obvious-type double patenting depends on establishing a *prima facie* of obviousness. From MPEP 2143.03: To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). From MPEP 2143.02: If the proposed modification or combination of the prior art would change the principle of operation of the prior art being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Claim 1, step (a), of the present application specifies specifying a time period. Claim 1 of U. S. Patent Number 6,813,691 specifies specifying a threshold. The examiner concludes with no support that a threshold is equivalent to a time period.

Claim 1, step (b), of the present application specifies evicting, from a cache memory, at least one entry that has remained unchanged for at least the time period. Claim 1 of U. S. Patent Number 6,813,691 specifies evicting, from a cache memory, at least one of the modified entries, when the number of modified entries in the cache memory exceeds the threshold. The examiner asserts with no support that evicting when an entry has remained unchanged for at least a time period is equivalent to evicting when the number of entries exceeds a threshold.

Furthermore, applicant submits that evicting after a time period is a different principle of operation than evicting when a number of entries exceeds a threshold. No *prima facie* case for obviousness has been established.

CLAIMS 1-8 IN LIGHT OF U.S. PATENT APPLICATION NUMBER 10/004,586.

Claim 1, steps (c)-(f) of the present application specifies: (c) measuring at least one performance parameter; (d) changing the value of the time period; (e) repeating steps (b) and (c); and (f) determining whether the performance parameter has changed. One step of

claim 1 of 10/004,586 specifies setting a bit to a second logical state. The examiner asserts with no support that setting a bit is equivalent to measuring a performance parameter, and the examiner provides no argument at all for any equivalence in 10/004,586 for steps (d)-(f) of claim 1 of the present application. No *prima facie* case for obviousness has been established.

CLAIM 1 IN LIGHT OF TALYANSKY *ET AL.*

From MPEP 2131:

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claim 1 specifies a method of improving performance of a computer system, comprising: (a) specifying a time period; (b) evicting, from a cache memory, at least one entry that has remained unchanged for at least the time period; (c) measuring at least one performance parameter; (d) changing the value of the time period; (e) repeating steps (b) and (c); and (f) determining whether the performance parameter has changed.

Talyansky *et al.* flush a dirty buffer that has remained unchanged for at least one sync period. Talyansky *et al.* do not teach or suggest changing the sync period, much less measuring a performance parameter before and after changing the sync period.

Regarding changing the sync period, the examiner cites Talyansky *et al.*, column 4, lines 41-60, stating that the cited text discusses two different sync periods. The cited text does not teach or suggest changing the sync period. The cited text merely states that figure 1 illustrates two syncs, one at t2 and one at t4. Changing of sync period is not discussed.

Regarding a performance parameter, the examiner cites column 3, lines 45-46. The cited lines state that the age of a dirty buffer is measured by sync periods. Effectively, the examiner is using a sync period both as the time period and as a measure of performance. Assuming for the sake of argument that the examiner is correct, then steps (c) – (f) require measuring the sync period, changing the sync period, flushing a buffer, measuring the sync period again, and determining whether the sync period changed. This is technically

meaningless, and is not taught or suggested by Talyansky *et al.*

CLAIMS 3-4 and 7-8 IN LIGHT OF TALYANSKY *ET AL.*

Claim 3 specifies measuring how many evicted entries are accessed during a predetermined time span. Talyansky *et al.* do not teach or suggest measuring how many evicted entries are accessed during a predetermined time span. Regarding claim 3, the examiner cites figure 1 and column 4, lines 41-60. There is no evicted entry that is accessed in the cited figure or text. In the office action dated 04/04/2005, at page 9, regarding claims 3-4 and 7-8, the examiner states: " . . . these claims are taught to the extent required by the actual limitations as the reference discusses evicting entries and optimizing or changing parameters." This broad statement, even if true, does meet the specificity required for a *prima facie* case of anticipation as discussed in MPEP 2131 *et seq.*

CONCLUSION

In view of the above, applicant respectfully requests that the examiner's rejection of claims 1-8 be reversed.

Respectfully submitted,

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CLAIMS APPENDIX

1. A method of improving performance of a computer system, comprising:

(a) specifying a time period;

(b) evicting, from a cache memory, at least one entry that has remained unchanged for at least the time period;

(c) measuring at least one performance parameter;

(d) changing the value of the time period;

(e) repeating steps (b) and (c); and

(f) determining whether the performance parameter has changed.

2. The method of claim 1, step (c) further comprising:

measuring the rate of cache-to-cache transfers.

3. The method of claim 1, step (c) further comprising:

measuring how many evicted entries are accessed during a predetermined time span.

4. The method of claim 1, step (b) further comprising:

evicting, from a cache memory, at least one modified entry that has remained unchanged for at least the time period.

5. The method of claim 1, step (b) further comprising:

evicting, from a cache memory, at least one entry that was received in a cache-to-cache transfer and has remained unchanged for at least the time period.

6. The method of claim 1, step (b) further comprising:

evicting, from a cache memory, at least one modified entry that was received in a cache-to-cache transfer and has remained unchanged for at least the time period.

7. The method of claim 1, further comprising:

repeating steps (a) through (f) until the performance parameter is optimized.

8. The method of claim 1, further comprising:

repeating steps (a) through (f) until the performance parameter change

EVIDENCE APPENDIX

Does not apply

RELATED PROCEEDINGS APPENDIX

None